Applicant: Riedl

Filed: September 30, 2005

Docket No.: I431.131.101/FIN421PCT/US

Title: DIFFUSION SOLDERED SEMICONDUCTOR DEVICE AND METHOD (As Amended)

IN THE CLAIMS

Please cancel claims 1-14 without prejudice.

Please add claims 15-29 as follows:

1-14. Cancelled

15. (New) A process for producing a semiconductor device, comprising:

coating a first side of a carrier with a first diffusion-soldering alloy;

coating a second side of the carrier with a second diffusion-soldering alloy wherein the melting points of diffusion-soldering alloys and diffusion-soldered joints are staggered in such a manner that a first melting point of the first diffusion-soldering alloy is lower than a second melting point of the second diffusion-soldering alloy, and the second melting point being lower than a third melting point of a first diffusion-soldered joint produced from the first diffusion-soldering alloy;

diffusion-soldering a first substrate to the first side of the carrier by heating the first diffusion-soldering alloy to the first melting point; and

diffusion-soldering a second substrate to the second side of the carrier by heating the second diffusion-soldering alloy to the second melting point.

16. (New) The process according to claim 15, wherein the first diffusion-soldering alloy is the composition Ga-yNi where 1% by weight < y < 20% by weight or Ga-xCu where 1% by weight < x < 40% by weight is applied to the first side, and the second diffusion-soldering alloy is the composition In-xAg where 1% by weight < x < 30% by weight or Sn-yAg where 1% by weight < y < 50% by weight is applied to the second side.

17. (New) The process according to claim 15, wherein the first diffusion-soldering alloy of the composition Ga-yNi where 1% by weight < y < 20% by weight or Ga-yAg where 1% by weight

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< y < 40% by weight is applied to the first side, and the second diffusion-soldering alloy of the composition In-xAg where 1% by weight < x < 30% by weight or Sn-yAg where 1% by weight < y < 50% by weight or Au-xSn where 5% by weight < x < 38% by weight, preferably where 10% by weight < x < 30% by weight, is applied to the second side.

18. (New) The process according to claim 15, wherein the diffusion-soldering alloy of the composition Ga-yAg where 1% by weight < y < 40% by weight is applied to the first side, and the diffusion-soldering alloy of the composition In-xAg where 1% by weight < x < 30% by weight or Sn-yAg where 1% by weight < y < 50% by weight or Au-xSn where 5% by weight < x < 38% by weight, preferably where 10% by weight < x < 30% by weight or Au-yGe where 4% by weight < y < 50% by weight, remainder Au, preferably where 7% by weight < y < 20% by weight, remainder Au, is applied to the second side.

19. (New) The process according to claim 15, wherein the first diffusion-soldering alloy of the composition In-xAg where 1% by weight < x < 30% by weight is applied to the first side, and the second diffusion-soldering alloy of the composition Sn-yAg where 1% by weight < y < 50% by weight or Au-xSn where 5% by weight < x < 38% by weight, preferably where 10% by weight < x < 30% by weight, or Au-yGe where 4% by weight < y < 50% by weight, remainder Au, preferably where 7% by weight < y < 20% by weight, remainder Au, is applied to the second side.

20. (New) The process according to claim 15, wherein the first diffusion-soldering alloy of the composition Sn-yAg where 1% by weight < y < 50% by weight is applied to the first side, and the second diffusion-soldering alloy of the composition Au-xSn where 5% by weight < x < 38% by weight, preferably where 10% by weight < x < 30% by weight, or Au-yGe where 4% by weight < y < 50% by weight, remainder Au, preferably where 7% by weight < y < 20% by weight, remainder Au, is applied to the second side.

21. (New) The process according to claim 16, wherein the first diffusion-soldering alloy of the

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composition Au-xSn where 5% by weight < x < 38% by weight, preferably where 10% by weight < x < 30% by weight, is applied to the first side, and the second diffusion-soldering alloy of the composition Au-yGe where 4% by weight < y < 50% by weight, remainder Au, preferably where 7% by weight < y < 20% by weight, remainder Au, is applied to the second side.

- 22. (New) The process according to claim 15, wherein a layer of silver, copper or nickel is applied to each side of at least one of the carrier or of the semiconductor chip prior to the application of the diffusion-soldering alloy.
- 23. (New) The process according to claim 15, wherein a layer of copper or a copper alloy is additionally applied prior to the application of the second diffusion-soldering alloy comprising Au-yGe where 4% by weight < y < 50% by weight, remainder Au, preferably where 7% by weight < y < 20% by weight, remainder Au.
- 24. (New) The process according to claim 15, wherein a layer of copper or silver or an alloy thereof is applied prior to the application of a diffusion-soldering alloy comprising Sn-yAg where 1% by weight < y < 50% by weight or Au-xSn where 5% by weight < x < 38% by weight, preferably where 10% by weight < x < 30% by weight.
- 25. (New) The process according to claim 15, wherein a layer sequence made up of aluminum and titanium is applied prior to the application of a diffusion-soldering alloy to the sides of a semiconductor chip.

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26. (New) A semiconductor device, comprising:

a semiconductor chip having a rear side and a top side with contact surfaces thereon,

a chip island having the rear side soldered thereto,

flat conductors soldered to the contact surfaces on the top side of the semiconductor chip, the soldered joints including different diffusion-soldering systems, with the first diffusion-soldering alloy on the rear side and with the second diffusion-soldering alloy on the top side, and the first and second diffusion-soldering alloys having different melting points.

27. (New) The semiconductor device according to claim 26, wherein a metal layer of copper or silver or nickel is between the diffusion-soldering alloy and the side of the semiconductor chip.

28. (New) The semiconductor device according to claim 26, wherein a layer sequence made up of aluminum and titanium is present on the sides of the semiconductor chip.

29. (New) The semiconductor device according to claim 23, wherein a layer sequence made up of aluminum and titanium is present on the sides of the semiconductor chip.